Code No: 155AK

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, January/February - 2023
COMPUTER ARCHITECTURE
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Convert 65.55 to IEEE 64 bit format.	[2]
b)	Compare Computer architecture and computer organization.	[3]
c)	What is mean by cache memory?	[2]
d)	List the different characteristics of memory system.	[3]
e)	What are the features of IA-32 processor?	[2]
f)	Write role of segment descriptor table.	[3]
g)	Write merits and demerits of pipelining.	[2]
h)	Write short notes on dynamic scheduling.	[3]
i)	Why pipelining in MIPS?	[2]
j)	Write features of DSP architecture.	[3]

PART – B

(50 Marks)

2.a) Enlist the advantages and disadvantages of Von Neumann's computer.
b) What is Instruction Type? Discuss in detail about various instruction formats. [5+5]

OR

3.a) Demonstrate steps to perform subtraction of unsigned numbers with an example.
b) With help of diagram, discuss multiple bus organization of a computer. [5+5]

4.a) Illustrate data transfer from input-output devices to CPU.
b) Define program interrupt? Explain types of interrupts occurred during execution of a program. [5+5]

OR

5.a) Draw and explain direct mapped cache organization.
b) Discuss in detail about auxiliary memory. [5+5]

6.a) Explain in detail about special purpose and segment IA-32 registers.
b) Illustrate the various instruction sets used for 8086 microprocessor. [5+5]

OR

7.a) List the various modes of operations in 80x86 microprocessor and explain each with suitable example.
b) Discuss in detail about input – output addressing in 80x86 processor. [5+5]

8.a) List and explain various types of array processors.

b) Differentiate Sequential record of execution and Instruction-level Parallel record of execution. [5+5]

OR

9.a) Discuss in detail about dynamic branch prediction with neat diagrams.

b) List and elaborate data hazards for ILP processors. [5+5]

10.a) Compare CISC, RISC, and VLIW architectures.

b) What is a Digital Signal Processor? With help of block diagram, explain how does Digital Signal Processor work? [5+5]

OR

11. Draw and explain multi-cycle implementation of MIPS. [10]

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